MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT

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The invention relates to microprocessor cards which are capable of performing operations on data supplied by memories associated with the microprocessor or by a terminal to which they are connected.

In a simplified manner, a microprocessor 10 (see single figure) comprises a central unit 12 which communicates with a program memory 16, a data memory 18 and a memory 14 of the RAM type, RAM being the English acronym for "Random Access Memory". This microprocessor 10 is connected to a terminal 20 by means of a link 32 and a contact pin 22.

The electrical signals applied by the terminal 20 to the contact pin 22 are analysed by the microprocessor 10 by means of a special so-called communication program recorded in the program memory 16, this communication program being adapted to the

communication protocol which controls the exchanges of information between the card and the terminal in both directions.

Analysis of the electrical signals applied to the contact pin 22 constitutes a relatively lengthy task for the central unit 12 ~~20~~, a task which mobilises a large part of the memories.

In a similar manner, the output of the information from the microprocessor 10 to the terminal 20 by means of the contact pin 22 also takes up the time of the central unit and space in the memories.

The aim of the present invention is therefore to produce a microprocessor card which does not have the aforementioned drawbacks so as to release time for the microprocessor for other tasks and to release memory capacity for these other tasks.

SUMMARY of the Invention

The invention lies in the fact that the communications between the terminal and the microprocessor card take place by means of a communication device, the said device being in the form of a hard-wired circuit.

The invention has the advantage of facilitating the development of a card and in particular reducing the qualification period and costs for it, the communication device, in the form of an independent part, being able to be qualified once and for all.

The invention relates to a microprocessor card with contacts, characterised in that the microprocessor communicates with the terminal by means of an

asynchronous communication device, the said communication device comprising:

- a circuit for analysing the electrical signals transmitted by the terminal so as to supply a series of electrical pulses,

- a circuit for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code indicating the status of the check,

- a circuit for determining each character from the pulses in the series,

- a first plurality of registers for recording the characters of the command and the address supplied by the character determination circuit and making them available to the microprocessor,

- a second plurality of registers for recording the characters of the data supplied by the character determination circuit and making them available to the microprocessor,

- a circuit for acknowledging the command, associated with the first plurality of registers, for analysing the characters of the command and supplying a code indicating the command reception status,

- a third plurality of registers for recording the codes for the data and for the status of execution of the command supplied by the microprocessor, and

- a circuit for transmitting to the terminal the codes supplied by the checking circuit, the command acknowledgement circuit and the third plurality of registers.

Brief Description of the Drawing

The invention will be understood more clearly by means of the following description of a particular example embodiment, the said description being given in relation to the accompanying drawing in which the single figure is a functional diagram of a microprocessor card having characteristics of the invention.

Detailed Description

As indicated in the introduction, a microprocessor card 30 of the prior art comprises essentially a microprocessor 10 connected to a terminal 20 by means of a bidirectional link 32, depicted in dotted lines, and a contact connector 22. The binary electrical signals applied by the terminal 20 to the contacts 22 are analysed directly by the microprocessor 10. In addition, the binary electrical signals supplied by the microprocessor 10 are transmitted to the terminal 20 by means of the connection 32 and contacts 22.

In such an architecture, the microprocessor 10 acts directly in the bidirectional communication process, which presents certain drawbacks, notably those disclosed in the introduction.

According to the invention, the bidirectional communication process is implemented by a communication device 40, disposed between the contact terminals 22 and the microprocessor 10.

The communication device 40 comprises:

- a circuit 34 for analysing the electrical signals applied by the terminal 20 to the contact terminal 22 of the card 30; this circuit 34 analyses

the electrical signals appearing on the contacts 22 so as to present them in the form of a series of electrical pulses of the binary type;

- a circuit 36 for checking the series of binary electrical pulses in order to determine the integrity of the series of electrical pulses, that is to say to check whether the series is complete in accordance with predetermined rules, for example by the use of a binary parity digit or a redundant code in the series; this checking circuit 36 supplies a binary signal or a binary code indicating the result of this check on a link 50;

- a circuit 38 for determining each character of the command or instruction, address or data item from the pulses in the series checked;

- a first plurality of registers 42 for recording on the one hand the characters of the command or instruction and on the other hand the characters of the address, as they are determined by the determination circuit 38;

- a second plurality of registers 44 for recording the characters of the data supplied by the determination circuit 38;

- a circuit 52 for acknowledging the command associated with the first plurality of registers 42 in order to analyse the characters of the command or instruction and to supply a signal or binary code indicating the terminal or the faulty reception of the command on a link 54,

- a third plurality of registers 46 for recording on the one hand the data supplied by the microprocessor 10 and on the other hand the status code indicating the statuses of execution of the command by the microprocessor 10, and

- a circuit 48 for transmitting, to the terminal 10 by means of the contacts 22, the signals and/or codes supplied by the checking circuit 36 on the link 50, by the acknowledgement circuit 52 on a link 54 and by the third plurality of registers 46 on a link 56.

The different circuits making up the communication device 40 are adapted to the communication protocol chosen. This communication protocol is of the asynchronous type and can be the one known by the name of RS232, with regard to a serial link habitually used between a so-called personal computer and its peripherals, or by the names V22, V23, etc with regard to connection by modem.

In order to check the integrity of the series of pulses, the terminal 20 must be designed to add redundant information to the signals transmitted, information whose presence the checking circuit 36 is capable of checking. It may be a case of the presence of a parity bit or binary digit or a redundant cyclic code. It should be noted that many communication protocols make provision for such a redundancy in order to check the integrity of the information transmitted. Where this check is not successful, the command is not executed and this decision is indicated by a code on the link 50.

This integrity check relates only to the succession of binary digits corresponding to the pulses in the series; the check on the command is carried out by the acknowledgement circuit 52 which determines that the command is complete and correct and indicates this on the link 54 by a particular code. In the event of an error, the circuit 52 can indicate this by another particular code. These particular codes are transmitted to the transmission circuit 48 but also to the character determination circuit 38 in order to indicate to it, in the event of correct acknowledgement, that the following characters are to be switched to the second plurality of registers 44 provided for recording the data transmitted by the terminal after the command if the latter has indeed been received in its entirety.